

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HAMID BAHRAMZADEH

Appeal No. 1997-0605
Application No. 08/551,981

ON BRIEF

Before BARRETT, HECKER, and DIXON, **Administrative Patent Judges**.
DIXON, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 13-19, which are all of the claims pending in this application.

We REVERSE.

BACKGROUND

The appellant's invention relates to a dual threshold digital receiver with large noise margin. An understanding of the invention can be derived from a reading of exemplary claim 13, which is reproduced below.

13. A method of converting one set of input signals of 0 and 3.3 volts, and another set of input signals of 0 and 2.5 volts into one set of output signals of 0 and 3.3 volts such that noise margin is maximized; said method being performed by a circuit having first and second transistors in series from a first bus at 3.3 volts to a second bus at 0 volts, and having third and fourth transistors in series from an output node between said first and second transistors to said second bus; said method including the steps of:

receiving said one set of input signals on an input which is coupled to respective gates in said first, second, and third transistors while a control signal of 0 volts is applied to a gate in said fourth transistor; and subsequently receiving said another set of input signals on said input while a control signal of 3.3 volts is applied to said gate in said fourth transistor;

selecting said transistors with respective turn-on voltages such that: a) said first and second transistors enter a fully-on state and said fourth transistor enters a fully-off state when said input signal is halfway to 3.3 volts and said control signal is at 0 volts; and, b) said first and fourth transistors enter said fully-on state and said second and third transistors enter a partially-on state when said input signal is half-way to said 2.5 volts and said control signal is at 3.3 volts;

further selecting said transistors with respective channel lengths and widths such that: a) said first, second and fourth transistors have respective channel resistances in said fully-on state of $R1_{ON}$, $R2_{ON}$ and $R4_{ON}$; b) said second and third transistors have respective channel resistances in said partially-on state of $R2_{PON}$ and $R3_{PON}$, both of which vary exponentially with gate voltage; and, c) $R2_{ON}$ equals $R1_{ON}$, and $R2_{PON}$ in parallel with $R3_{PON}$ plus $R4_{ON}$ equals $R1_{ON}$.

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The prior art references of record relied upon by the examiner¹ in rejecting the appealed claims are:

Konishi	4,533,841	Aug. 06, 1985
Yoshino	5,019,725	May 28, 1991

Claims 13-19 stand rejected under 35 U.S.C. § 103 as being unpatentable over Konishi in view of Yoshino.

Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellant regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 15, mailed Sep. 4, 1996) for the examiner's reasoning in support of the rejections, and to the appellant's brief (Paper No. 14, filed July 29, 1996) and reply brief (Paper No. 16, filed Sep. 16, 1996) for the appellant's arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellant's specification and claims, to the applied prior art references, and to the respective positions articulated by the appellant and the examiner. As a consequence of our review, we make the determinations which follow.

¹ The examiner lists Wanlass U.S. Patent No. 5,216,299, in the prior art of record, but does not include this reference in the statement of the rejection. Therefore, this reference forms no part of our consideration.

Rejections based on § 103 must rest on a factual basis with these facts being interpreted without hindsight reconstruction of the invention from the prior art. The examiner may not, because of doubt that the invention is patentable, resort to speculation, unfounded assumption or hindsight reconstruction to supply deficiencies in the factual basis for the rejection. **See *In re Warner***, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), ***cert. denied***, 389 U.S. 1057 (1968). Our reviewing court has repeatedly cautioned against employing hindsight by using the appellants' disclosure as a blueprint to reconstruct the claimed invention from the isolated teachings of the prior art. **See, e.g., *Grain Processing Corp. v. American Maize-Products Co.***, 840 F.2d 902, 907, 5 USPQ2d 1788, 1792 (Fed. Cir. 1988). Since all the limitations of independent claims 13 are neither taught nor suggested by the applied prior art in the reconstructed combination, we cannot sustain the examiner's rejection of independent claims 13 and 14 under 35 U.S.C. § 103.

Appellant argues that the prior art to Konishi does not teach or suggest the last two clauses of claims 13 and 14 with respect to selecting the transistors. (See brief at page 5.) We agree with appellant. The examiner equates the selection of the transistors and their resistances to be merely a design expedient for a skilled artisan. (See answer at pages 4 and 5.) The examiner relies upon Yoshino to provide a teaching concerning the threshold and the relationship between the width and length of transistors. We agree with

the examiner that the basic elements of the claimed invention were known in the art at the time of the invention, but in our view, the examiner has not provided any evidence why one skilled in the art would have been motivated to select transistors with the operation relative to a threshold and relative channel resistances as recited in the last two clauses of claim 13, irrespective of the specific numeric values 0, 2.5 and 3.3. The examiner has equated the value of the threshold voltage and the input/output voltages to be a "design expedient" and maintains that the resistances could be met simply by selecting the W/L ratio of the channel sizes. (See answer at pages 4 and 5.) We disagree with the examiner. While certain features of the claimed invention, may individually be deemed to be design expedients for skilled artisans, the examiner goes well beyond any individual feature in rationalizing the obviousness of the claimed invention. In our view, the examiner has essentially maintained that the method of selection and use of specific circuit components within the disclosed circuit of Konishi is *per se* obvious because Yoshino teaches that it was known that W/L ratios may vary the operation of transistors. We disagree with the examiner. In our opinion, the examiner is not relying upon knowledge from the prior art, but upon knowledge of the invention which was gleaned from appellant's own specification to provide the motivation for the selecting values and operating the circuit in the manner claimed. Therefore, we cannot sustain the rejection of independent claims 13 and 14 and their dependent claims 15-19.

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CONCLUSION

To summarize, the decision of the examiner to reject claims 13-19 under 35 U.S.C. § 103 is reversed.

REVERSED

LEE E. BARRETT
Administrative Patent Judge

STUART N. HECKER
Administrative Patent Judge

JOSEPH L. DIXON
Administrative Patent Judge

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